THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GEORGE B. TUMA, and WADE B. TUMA

Appeal No. 1997-4314
Application No. 08/155,332[1]

ON BRIEF

Before HAIRSTON, KRASS, and FRAHM, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 6 and 8 through 11, all of the pending claims.

[1] Application for patent filed November 19, 1993.

The invention is directed to an address generator for a memory device. In particular, a dedicated multiplier circuit for calculating the desired starting address of a read or write memory operation is included in a disk drive's address generator. As it receives data block numbers, the multiplier circuit multiplies the data block number by a block size value to quickly generate the physical address. The block size value is programmable.

Representative independent claim 1 is reproduced as follows:

1. An address generator for a memory device, the address generator connecting to a computer peripheral bus and providing an address to a memory array, the address generator comprising:

an input port connectable to the computer peripheral bus;

a multiplier circuit operatively connected to the input port and receiving two multiplicands from the port, a first multiplicand being a block number and a second multiplicand being a programmable block length value, the multiplier circuit providing a product of the two multiplicands; and

an output port operatively connected to the multiplier and receiving the product, the output port being connected to the memory array.

The examiner relies on the following references:

Takasaki et al. (Takasaki) 5,088,031 Feb. 11, 1992
Cassidy et al. (Cassidy) 5,343,426 Aug. 30, 1994
(filed Jun. 11, 1992)

Claims 1 through 6 and 8 through 11 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner offers Takasaki with regard to claims 1 through 4 and 8 through 11, adding Cassidy with regard to claims 5 and 6.

Reference is made to the brief and answer for the respective positions of appellants and the examiner.

OPINION

Turning first to the rejection of independent claims 1 and 9, the examiner contends that Takasaki discloses an address generator for a memory device as a translation circuit 50A in Figure 7 and that the reference teaches a multiplier circuit that receives two multiplicands and provides the product, referring to column 9, line 29 of the reference. The examiner admits that Takasaki does not specifically teach that the second multiplicand is “programmable” but the examiner contends that it is “common knowledge” that any input signal into a computer “could easily be changed/programmed into a

device" [answer-page 3]. Thus, the examiner concludes that it would have been obvious to make the block length programmable by an external source so its value can be easily controlled. The examiner also states that Takasaki "inherently" teaches an input port by any line which connects the multiplier to the input source. The examiner also realizes that Takasaki does not teach an input port connected to a peripheral bus but contends that it would have been obvious to connect the input port to a peripheral bus "because this would let the peripheral bus supply the multiplicands from any source connected to the bus" [answer-page 4].

For their part, appellants contend that Takasaki does not suggest a "programmable" block length value, as claimed. We disagree. We do not countenance the examiner's contention that it is common knowledge that any input signal "could" be programmed into a computer because this is not the proper test for obviousness under 35 U.S.C. § 103. Merely because something "could" be done does not, necessarily make it obvious to do so. However, as broadly recited in independent claims 1 and 9, "programmable" block length value merely indicates the ability to input a block length value. As can

be seen in Figure 7 and column 9, lines 36 et seq, of Takasaki, a block length value is put into LBN register 51 as a parameter. While it may be, as appellants explain at page 8 of the brief, that Takasaki is concerned with different logical block lengths for different machines, i.e., one value for each machine, rather than appellants' programmable logical block number for any one machine, the fact that Takasaki's LBN register 51 can be loaded initially with a block length value, even if it is only one value for each machine, makes that register "programmable," as broadly claimed, because the LBN register can be said to have been "programmed" with that one value. [Note, infra, the different result reached with regard to claim 10].

Appellants further contend that Takasaki does not suggest the claimed "input port connectable to the computer peripheral bus," pointing out that Takasaki does not disclose a peripheral bus, or any bus, because Takasaki is directed to a virtual machine that does not contain any physical bus. However, we agree with the examiner that the data flow lines in Takasaki are suggestive of buses. The skilled artisan adapting Takasaki's device for non-virtual machine

environments would clearly have supplied data over a peripheral bus to an input port

With regard to claims 10 and 11, appellants contend that these claims are more specific as to the programmability feature. We agree. With regard to claim 10, Takasaki clearly does not suggest anything related to changing the block size value "in response to a mode command" because LBN register 51 does not appear to be "programmable" in that sense. However, we disagree with appellants as to claim 11 since this claim merely calls for broadly "programming" the block length value into the input port. As stated supra, the setting of a value into LBN register 51 is a form of "programming" and it would have been clear to artisans that this is to be done through some type of "input port."

Since appellants do not specifically argue any other claims, the examiner's decision is affirmed as to claims 1 through 6, 8, 9 and 11 but is reversed as to claim 10.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON Administrative Patent Judge	)	
ERROL A. KRASS Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
ERIC FRAHM Administrative Patent Judge	)	

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